

REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 2, 3, 5-8, 10-23, 26-30 and 32-43 are in this case. Claims 18-22 and 37 have been rejected under § 112, first paragraph. Claims 23 and 38 have been rejected under § 112, second paragraph. Claims 2, 3, 5-8, 10-23, 26-30 and 32-43 have been rejected under § 103(a). Dependent claims 5, 39 and 43 have been canceled. Independent claims 23, 26, 29 and 33 have been amended. New dependent claims 44-47 have been added.

The claims before the Examiner are directed toward methods of assembling and testing electronic devices, specifically, systems-in-package (SIPs), and to a device so assembled and tested. A CPU (in some embodiments, only one CPU), a nonvolatile memory and a volatile memory are fabricated on respective, physically independent chips and are packaged together in a common package with the CPU operationally connected to the memories. Testing programs, for testing the memories by writing to the memories, are stored in the nonvolatile memory and are executed by the CPU from the volatile memory to test the memories. Then the CPU is tested. The results of the tests of the memories are stored in the nonvolatile memory. In some embodiments, the testing of the CPU includes reading the results of testing the memories.

§ 112, First Paragraph Rejections

The Examiner has rejected claims 18-22 and 37 under § 112, first paragraph, as being indefinite for failing to comply with the enablement requirement. Specifically, the Examiner proposes that the specification does not enable testing the

nonvolatile memory by writing to the nonvolatile memory, as recited in claim 18. Claims 19-22 and 37 have been rejected similarly by virtue of depending from claim 18.

The Examiner's rejection is respectfully traversed. Testing a memory by writing to the memory is taught, as a part of the testing of a prior art SIP, on page 2 lines 8-11 of the specification:

By contrast, a memory chip typically has a small number of external connectors to test, but the test may take upwards of ten minutes because each bit of the memory chip must be tested by writing to the bit and then reading the bit. (emphasis added)

That the memory chip of a SIP may be a nonvolatile memory chip is stated on page 1 lines 19-22 of the specification:

...a processor for controlling a cellular telephone could include a central processing unit (CPU), a nonvolatile memory such as a flash memory and a volatile memory such as a SDRAM, each fabricated on its own chip, and all packaged in the same package. Such a system is called a "System-in-Package" (SIP)... (emphasis added)

It is implicit that the present invention would test its nonvolatile memory similarly.

§ 112, Second Paragraph Rejections

The Examiner has rejected claims 23 and 38 under § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, the Examiner has pointed out that it is not clear, in claim 23 if the first testing program is stored in the nonvolatile memory or elsewhere on the first chip. Claim 38 has been rejected similarly by virtue of depending from claim 23.

Claim 23 now has been amended to clarify that the first testing program is stored in the nonvolatile memory. Support for this amendment is found in the specification in the Figure, that shows program A stored in flash memory 14.

§ 103(a) Rejections – Chesley ‘142 in view of AAPA and further in view of

Ledford et al., ‘056

The Examiner has rejected claims 2, 3, 5, 26, 27, 29, 33, 34, 40 and 43 under § 103(a) as being unpatentable over Chesley, US Patent No. 4,333,142 (henceforth, “Chesley ‘142”) in view of Applicant Admitted Prior Art (henceforth, “AAPA”) and further in view of Ledford et al., US Patent No. 6,347,056 (henceforth, “Ledford et al. ‘056”). Applicant presumes that the Examiner intended to also reject claim 39 as unpatentable over Chesley ‘142 in view of AAPA and further in view of Ledford et al. ‘056, and not as unpatentable over Chesley ‘142 in view of AAPA, because claim 39 depends from claims 26. The Examiner’s rejection is respectfully traversed.

Claims 5, 39 and 43 has been canceled, thereby rendering moot the Examiner’s rejection of these claims.

Chesley ‘142 teaches a computer and memory system fabricated on a single wafer **11** with redundant components and configured to test itself when power is applied to identify and not use inoperative components. Specifically, the system includes many CPU modules **12**, many ROM modules **13** and many RAM modules **14**. When power is applied to the system, each CPU tests itself until a working CPU is found. The working CPU does checksum testing of the ROMs until a working ROM is found. The working CPU then runs a copy of a CPU test routine that stored in the working ROM to test itself and also runs a copy of a RAM test routine that is stored in the working ROM to test the RAMs in order to identify working RAMs.

AAPA is cited by the Examiner only to show that it is known to fabricate a CPU and one or more memories on separate chips and to assemble and package the chips in a SIP. Ledford et al. ‘056 is cited only to show that it is known to store the

results of testing a nonvolatile memory in the nonvolatile memory itself. Therefore, the following remarks focus on Chesley '142.

Independent claims 26 and 33 have been placed in condition for allowance by the inclusion therein of the limitations that the chip on which the CPU is fabricated has only one such CPU fabricated thereon and that that CPU is the only CPU in the package. Support for these amendments is found in the specification in the Figure that shows CPU chip **12** as the only CPU chip in SIP **10**. It is implicit, in light of page 1 lines 19-22,

For example, a processor for controlling a cellular telephone could include a central processing unit (CPU), a nonvolatile memory such as a flash memory and a volatile memory such as a SDRAM, each fabricated on its own chip, and all packaged in the same package. Such a system is called a "System-in-Package" (SIP)... (emphasis added)

that, like the prior art SIP discussed in this citation from page 1 lines 19-22, SIP **10** has only one CPU fabricated on its CPU chip **12**.

It follows that the CPU recited in claims 26 and 33 as now amended is the only CPU that is packaged along with the memories and that is operationally connected to the memories. Chesley '142 teaches explicitly against having only one CPU module **12** in his computer and memory system on wafer **11**, in column 1 lines 13-29:

Computer systems are commonly created by interconnecting smaller modules such as CPU's, memory modules, and input/output controllers...

In recent years, large scale integration (LSI) has been developed to the point where the modules can be integrated on a single chip, e.g., microprocessor CPUs...However, a potential problem exists because a bad LSI module can cause the entire wafer computer system to malfunction. Thus, redundant modules must be present on the wafer... (emphasis added)

In particular, in the system of Chesley '142 (column 2 lines 8-13),

The system includes a plurality of CPU modules 12, ROM modules 13 and RAM modules 14. In the embodiment illustrated, four CPU modules and four ROM modules are provided, although a greater or lesser degree of redundancy can be provided if desired.

But in any case, according to Chesley '142, *some* degree of redundancy must be provided.

The "single CPU" limitation in claims 26 and 33 as now amended renders dependent claims 39 and 43 redundant. Therefore, claims 39 and 43 have been canceled. With independent claims 26 and 33 in condition for allowance in their present form it follows that claims 27 and 34 that depend therefrom also are allowable.

Claim 29 has been placed in condition for allowance by the inclusion therein of the limitations of claim 5. Correspondingly, claim 5 has been canceled.

As stated in MPEP 2143.03,

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Neither Chesley '142 nor AAPA nor Ledford et al. '056 teach testing a CPU by reading results of testing of memories, by that CPU, that are stored in one of the memories tested by that CPU. Ledford et al. '056 deals only with testing memories. Applicant's admitted prior art, with regard to testing a CPU in a SIP, is that (page 2 lines 1-2)

A SIP is tested much as an individually packaged chip is tested:
by being mounted on a testing board...

In other words, according to Applicant's admitted prior art, the CPU and the memories of a SIP are tested separately on a testing board. Chesley '142 stores testing results in tested memories, insofar as (column 3 lines 50-52)

...a table of the addresses of the good and bad RAM's is created in the first good RAM

but the testing of CPUs 12 by Chesley '142 does not include reading that table. Indeed, Chesley '142 tests CPUs 12 before ever testing any RAMs 14, as stated in column 3 lines 47-49:

Once a good ROM and a good CPU are found, the CPU uses a RAM test routine contained in the ROM to test each RAM module in sequence. (emphasis added)

With independent claim 29 allowable in its present form it follows that claims 2, 3 and 40 that depend therefrom also are allowable.

§ 103(a) Rejections - Chesley '142 in view of AAPA

The Examiner has rejected claims 7, 8, 10-16, 18-21, 23, 30, 32, 36-39, 41 and 42 under § 103(a) as being unpatentable over Chesley '142 in view of AAPA. As noted above, Applicant presumes that the Examiner intended to reject claim 39 as unpatentable over Chesley '142 in view of AAPA and further in view of Ledford et al. '056, and not as unpatentable over Chesley '142 in view of AAPA, because claim 39 depends from claims 26 that was rejected as unpatentable over Chesley '142 in view of AAPA and further in view of Ledford et al. '056. The Examiner's rejection is respectfully traversed.

As noted above, according to MPEP 2143.03, in order for *prima facie* obviousness of a claim to be established, all the claim limitations must be taught or suggested by the cited references. This is not the case with regard to independent claims 7, 30 and 32. Specifically, the prior art cited by the Examiner fails to teach or suggest steps (e) and (f) of claim 7, steps (d) and (e) of claim 30 and steps (e) and (f) of claim 32: loading a testing program into the volatile memory and testing one of the memories (claims 7 and 32) or testing the volatile memory (claim 30) by using the

CPU to execute the loaded program. A CPU module **12** of Chesley '142 tests a ROM module **13** by summing the words of the ROM module **13** and comparing the sum to a checksum stored in the ROM module **13**. The check sum routine that the CPU module **12** executes is "permanently built into the logic of each CPU" (column 3 lines 15-16). A CPU module **12** of Chesley '142 tests a RAM module **14** by executing a RAM test program that is stored in a ROM module **13**. As best understood, both the check sum routine and the RAM test program are executed in place and are not loaded into a RAM module **14** for execution. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about how the memories are tested.

Similar arguments were presented in response to the Office Action mailed July 14, 2006. In the Office Action mailed December 29, 2006, the Examiner directed Applicant's attention to column 3 lines 17-28 of Chesley '142 and commented:

Here the RAM is the volatile memory and when the CPU uses line 26 to "WRITE" on to the RAM it is in an essence loading the test program.

Applicant responded by pointing out that, as best understood, the purpose of line **26** is to write data to a RAM module **14** during normal operation of the computer of Chesley '142 after the good RAM modules **14** have been found, as described in column 3 lines 55-58:

The RAM's are utilized as a page allocated memory system in which data and program space is allocated on demand on a page basis, with each RAM module corresponding to one page.

There is neither a hint nor a suggestion in Chesley '142 of loading any code from a ROM module **13** to a RAM module **14** for execution. In particular, the check sum routine cannot be loaded into a RAM module **14** for execution because the check sum

routine is executed *only* to test ROM modules 13 *before* any RAM modules 14 are accessed. As stated in column 3 lines 47-49,

Once a good ROM and a good CPU are found, the CPU uses a RAM test routine contained in the ROM to test each RAM module in sequence. (emphasis added)

The Examiner now has responded to these arguments as follows:

As per the contention that Chesley does not teach loading a test program into the volatile memory Examiner would like to respectfully state that “loading a test program” is a broad limitation that given the write capabilities of RAM it is not possible that the RAM is being tested without any instructions being loaded onto the RAM. Chesley mentions that the module to test the RAM is on the ROM, in order to test the write capabilities of RAM Chesley will have to load some instructions from the ROM, further the address comparator on the RAM will be given an address from the CPU for comparison. Therefore, it is not possible that Chesley is testing the RAM without loading a testing program onto the RAM.

Applicant respectfully disagrees. The RAM test program *must* be executable in place because when Chesley ‘142 tests his first RAM module 14 he does not yet know whether that RAM module 14 is a good RAM module 14. What Chesley ‘142 writes to a RAM module 14 to test that RAM module 14 are not *instructions* that are executed by the CPU module 12 that does the testing, but *data*. Not even an address that the CPU module 12 gives the address comparator on the RAM module 14 can be construed as an instruction that is executed *by the CPU module 12* from the RAM module 14. Therefore, even construed broadly, the limitation that the CPU tests a memory by executing a program that has been loaded into the volatile memory (claim 7 element (f), claim 30 element (e), claim 32 element (f)) is lacking in Chesley ‘142.

With independent claims 7, 30 and 32 allowable in their present form it follows that claims 8, 10-16, 36, 41 and 42 also are allowable.

Although claim 13 is allowable merely by virtue of depending from claim 7, Applicant respectfully points out that claim 13 also is allowable for the reasons presented above in defense of claim 29 as now amended.

Turning now to independent claims 18 and 23, as noted above, according to MPEP 2143.03, in order for *prima facie* obviousness of a claim to be established, all the claim limitations must be taught or suggested by the cited references. In the case of claims 18 and 23, the limitation that is lacking in the cited prior art is the limitation, recited in claim 18 step (d) and claim 23 element (a), that the program for testing the nonvolatile memory is included in the nonvolatile memory itself. In Chesley '142 the check sum routine that the CPU module 12 executes to test ROM modules 13 is "permanently built into the logic of each CPU" (column 3 lines 15-16). ROM modules 13 store only CPU test programs and RAM test programs. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about how the memories are tested.

Similar arguments were presented in response to the Office Action mailed July 14, 2006. In reply, the Examiner directed Applicant's attention to column 3 lines 7-14 of Chesley '142 and commented:

Here, the ROM is the non-volatile memory, and the CPU is performing a "test function" to test the ROM. The ROM "contains" test program and check sum, which are used to test the ROM.

Applicant responded by pointing out that the ROM contains the check sum but not the test program. As noted above, the check sum routine is "permanently built into the logic of each CPU" (column 3 lines 15-16).

The Examiner now has responded to these arguments as follows:

As per the contention that Chesley does not teach storing a test program on the nonvolatile memory, the Examiner would like to

respectfully cite “Each **ROM module contains** an identical copy of a CPU and RAM test program as well as **other desired service routines**, with the addresses shifted to reflect the proper module addresses. In addition, **the last word of each ROM module contains** a check sum of all of the other words of the module so that a CPU can perform a simple test function, in this case summation, upon all words of the ROM to verify that the ROM is operating correctly.” Examiner contends that storing a test program on the nonvolatile memory is a broad limitation and the last word of each ROM module, which is used to test the ROM and other desired service routines, which are both contained in the ROM teach a test program being stored on a nonvolatile memory. (emphasis in original)

Applicant understands the Examiner to be making two points here:

1. The “other desired service routines” could include a ROM test program.
2. In any case, the check sum that is stored in a ROM module **13** is a part of the check sum test routine.

With regard to the first point, just as a RAM test program should not be executed from a RAM module **14** that is not known to be reliable, so a ROM test program should not be executed from a ROM module **13** that is not known to be reliable. Therefore, one skilled in the art who uses the methodology of Chesley ‘142 would not include among the “other desired service routines” a test program for testing the ROM module **13** in which those service routines are stored.

With regard to the second point, even though a claim is given its “broadest reasonable interpretation”, as stated in MPEP 2111,

The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999)

In the present case, those skilled in the art would expect a test “program” to consist of instructions that are executed by the CPU module **12** that tests the ROM module **13**, and not a checksum word that is stored in the ROM module **13**. Claim 18 recites the step (step (e)) of “executing said program, by said CPU”. In what sense does a CPU

“execute” a checksum? Those skilled in the art would consider a pre-stored “checksum word” of a ROM module and an “executable test program” for computing the checksum word to be separate and distinct aspects of a ROM test mechanism.

With independent claims 18 and 23 allowable in their present form it follows that claims 19-21, 37 and 38 that depend therefrom also are allowable.

Nevertheless, in order to make explicit the broadest reasonable interpretation of the term “program” in claims 18 and 23, new claims 46 and 47 have been added. New claim 46 adds to claim 18 the limitation that the program includes executable code. New claim 47 adds to claim 23 the limitation that the first testing program includes executable code. Support for new claims 46 and 47 is found in the specification on page 8 lines 9-12:

First, CPU chip 12 loads program A from flash memory chip 14 into SDRAM chip 16, executes program A in SDRAM chip 16 to test flash memory chip 14, and stores the results of the test in flash memory chip 14. (emphasis added)

It is inherent that a program A that is “executed” includes executable code.

New claims 44 and 45 have been added to add a similar limitation to claims 10 and 14. New claims 44 and 45 also recite the limitation that the testing program is for testing the nonvolatile memory. Support for the latter amendment is found in the specification *inter alia* in the above citation from page 8 lines 9-12: program A is for testing flash memory chip 14.

§ 103(a) Rejections - Chesley ‘142 in view of AAPA and Ledford et al., ‘056, and further in view of Takizawa ‘663

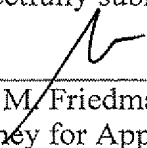
The Examiner has rejected claims 6, 17, 22, 28 and 35 under § 103(a) as being unpatentable over Chesley ‘142 in view of AAPA and Ledford et al. ‘056, and further

in view of Takizawa, US Patent No. 6,198,663. The Examiner's rejection is respectfully traversed.

It is demonstrated above that independent claims 7, 18, 26, 29 and 33 are allowable in their present form. It follows that claims 6, 17, 22, 28 and 35 that depend therefrom also are allowable.

In view of the above amendments and remarks it is respectfully submitted that independent claims 7, 18, 23, 26, 29, 30, 32 and 33, and hence dependent claims 2, 3, 5, 6, 8, 10-17, 19-22, 27, 28, 34-38, 40-42 and 44-47 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,



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